1. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element circuit fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

a conductive layer provided on a back side of said substrate.

2. The semiconductor device of claim 1, wherein said electrical element comprises at least one electrical element selected from the group consisting of transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

3. The semiconductor device of claim 1, wherein said conductive layer is electrically coupled to a terminal supplying said bias voltage.

4. The semiconductor device of claim 1 further comprising a plurality of conductive plugs for respectively coupling said bias voltage source to said distribution regions.

5. The semiconductor device of claim 1, wherein said conductive layer comprises a conductive metallic layer.

6. The semiconductor device of claim 5, wherein said conductive metallic layer has a thickness of less than or equal to 10 mil.

7. The semiconductor device of claim 5, wherein said conductive metallic layer is secured to the backside of said substrate with a conductive adhesive.

8. The semiconductor device of claim 5, wherein said conductive metallic layer is electrically coupled to a terminal supplying said bias voltage.

9. The semiconductor device of claim 5, wherein said conductive metallic layer has a resisitivity less than 1×10^{-8} Ohm-meter.

10. The semiconductor device of claim 5, wherein said conductive metallic layer comprises at least one material selected from the group consisting of copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

11. The semiconductor device of claim 10, wherein said conductive metallic layer is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

12. The semiconductor device of claim 5, wherein said metallic layer has at least one length which exceeds a length of said substrate.

13. The semiconductor device of claim 1, wherein said conductive layer comprises a cured conductive paste.

14. The semiconductor device of claim 13, wherein said conductive paste has a thickness of less than or equal to 1 mil.

15. The semiconductor device of claim 13, wherein said conductive paste has a resistivity less than 1×10^{-5} Ohm-meter.

16. The semiconductor device of claim 13, wherein said conductive paste comprises a material with conductive particles therein.

17. The semiconductor device of claim 16, wherein said conductive particles comprise at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

18. The semiconductor device of claim 1, wherein said conductive layer comprises an isotropically conductive polymeric film.

19. The semiconductor device of claim 18, wherein said conductive polymeric film has a thickness greater than 1 mil.

20. The semiconductor device of claim 18, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

21. The semiconductor device of claim 18, wherein said conductive polymeric film comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

22. The semiconductor device of claim 1, wherein said conductive layer comprises a conductive metallic film.

23. The semiconductor device of claim 22, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

24. The semiconductor device of claim 22, wherein said conductive metallic film has a resistivity less than 1 x 10^{-5} Ohm-meter.

25. The semiconductor device of claim 22, wherein said conductive metallic film comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

26. The semiconductor device of claim 25, wherein said conductive metallic film is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

27. The semiconductor device of claim 1, wherein said device is a memory device.

28. The semiconductor device of claim 27, wherein said memory device is a dynamic random access memory (DRAM) device.

29. The semiconductor device of claim 1, wherein said device is a logic device.

30. The semiconductor device of claim 1, wherein said device is a processor device.

31. A method of forming a semiconductor device, said method comprising:

fabricating at least one electrical element on an upper side of a semiconductor substrate;

fabricating a plurality of bias voltage distribution regions over said upper side of said substrate for receiving a bias voltage and applying said bias voltage to said substrate; and

securing a conductive layer to a backside of said substrate.

32. The method of claim 31, wherein said electrical element comprises at least one electrical element selected from the group consisting of transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

33. The method of claim 31, wherein said conductive layer comprises a conductive metallic layer.

34. The method of claim 33, said conductive metallic layer has a thickness of less than or equal to 10 mil.

35. The method of claim 33, wherein said conductive metallic layer is secured to said substrate backside with a conductive adhesive.

36. The method of claim 33, further comprising coupling said conductive metallic layer to a terminal for supplying said bias voltage.

37. The method of claim 33, wherein said conductive metallic layer has a resisitivity less than between 1 x 10^{-8} Ohm-meter.

38. The method of claim 33, wherein said conductive metallic layer comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al)

39. The method of claim 38, wherein said conductive metallic layer is formed of as least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

40. The method of claim 33, wherein said conductive metallic layer has at least one length which exceeds a length of said substrate.

41. The method of claim 33, wherein said conductive metallic layer is applied to said substrate back side after a fabricated wafer is cut into individual semiconductor devices.

42. The method of claim 31, further comprises providing a plurality of conductive plugs for respectively coupling a received bias voltage source to said distribution regions.

43. The method of claim 31, wherein said conductive layer comprises a cured conductive paste.

44. The method of claim 43, wherein said conductive paste has a thickness less than or equal to 1 mil.

45. The method of claim 43, wherein said conductive paste has a resistivity less than 1 x 10^{-5} Ohm-meter.

46. The method of claim 43, wherein said conductive paste is formed of a material comprising conductive particles.

47. The method of claim 43, wherein said conductive paste comprises conductive particles selected from at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

48. The method of claim 43, further comprising applying said conductive paste to the backside of a fabricated wafer after the wafer is background and before the wafer is cut into individual semiconductor devices.

49. The method of claim 31, wherein said conductive layer comprises an isotropically conductive polymeric film.

50. The method of claim 49, wherein said conductive polymeric film has a thickness greater than about 1 mil.

51. The method of claim 49, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

52. The method of claim 49, wherein said conductive polymeric film comprises conductive particles selected from at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

53. The method of claim 49, further comprising applying said conductive polymeric film to the backside of a fabricated wafer after said wafer is background and before said wafer is cut into individual semiconductor devices.

54. The method of claim 49, wherein said conductive polymeric film is applied at a temperature greater than about 175 degrees Celsius.

55. The method of claim 49, wherein said conductive polymeric film is pressed against said substrate at a pressure greater than 1 mega Pascal.

56. The method of claim 31, wherein said conductive layer comprises a conductive metallic film.

57. The method of claim 56, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

58. The method of claim 56, wherein said conductive metallic film has a resistivity less than 1×10^{-5} Ohm-meter.

59. The method of claim 56, wherein said conductive metallic film comprises conductive particles selected from at least one the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

60. The method of claim 56, further comprising applying said conductive metallic film to the backside of a fabricated wafer after said wafer is background and before said wafer is cut into individual semiconductor devices.

61. The method of claim 56, wherein said conductive metallic film is deposited by a method selected from the group consisting of: electroless plating, electrolytic plating, molecular beam epitaxy (MBE), vapor phase epitaxy (VPE), physical vapor deposition (PVD), chemical vapor deposition (CVD) and metal organic chemical vapor deposition (MOCVD).

62. The method of claim 31, wherein said device is a memory device.

63. The method of claim 62, wherein said memory device is a dynamic random access memory (DRAM) device.

64. The method of claim 31, wherein said device is a logic device.

65. The method of claim 31, wherein said device is a processor device.

66. A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

a conductive layer provided on a back side of said substrate.

67. The system of claim 66, wherein said electrical element comprises at least one electrical element selected from the group consisting of: transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

68. The system of claim 66, wherein said conductive layer is electrically coupled to a terminal supplying said bias voltage.

69. The system of claim 66, further comprising plurality of conductive plugs for respectively coupling said bias voltage to said distribution regions.

70. The system of claim 66, wherein said conductive layer comprises a conductive metallic layer.

71. The system of claim 70, wherein said conductive metallic layer has a thickness of less than or equal to 10 mil.

72. The system of claim 70, wherein said conductive metallic layer is secured to the backside of said substrate with a conductive adhesive.

73. The system of claim 70, wherein said conductive metallic layer is electrically coupled to a terminal for supplying said bias voltage.

74. The system of claim 70, wherein said conductive metallic layer has a resisitivity less than 1×10^{-8} Ohm-meter.

75. The system of claim 70, wherein said conductive metallic layer comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

76. The system of claim 75, wherein said conductive metallic layer is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

77. The system of claim 70, wherein said conductive metallic layer has a length which exceeds a length of said substrate.

78. The system of claim 66, wherein said conductive layer comprises a cured conductive paste.

79. The system of claim 78, wherein said conductive paste has a thickness of less than or equal to 1 mil.

80. The system of claim 78, wherein said conductive paste has a resistivity less than 1 x 10^{-5} Ohm-meter.

81. The system of claim 78, wherein said conductive paste comprises a resin with conductive particles.

82. The system of claim 81, wherein said conductive paste comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

83. The system of claim 66, wherein said conductive layer comprises an isotropically conductive polymeric film.

84. The system of claim 83, wherein said conductive polymeric film has a thickness greater than 1 mil.

85. The system of claim 83, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

86. The system of claim 83, wherein said conductive polymeric film comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

87. The system of claim 66, wherein said conductive layer comprises a conductive metallic film.

88. The system of claim 87, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

89. The system of claim 87, wherein said conductive metallic film has a resistivity less than 1×10^{-5} Ohm-meter.

90. The system of claim 87, wherein said conductive metallic film comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

91. The system of claim 90, wherein said conductive metallic film is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

92. The system of claim 66, wherein said device is a memory device.

93. The system of claim 92, wherein said device is a dynamic random access memory (DRAM) device.

94. The system of claim 66, wherein said device is a logic device.

95. The system of claim 66, wherein said device is a processor device.

96. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate; and

a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and at least one non-substrate area of said device.

97. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source.

98. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate;

a conductive metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said semiconductor device; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device.

99. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

a conductive layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device.